SAMPLE QUESTIONS

F.Y.B.Sc. I.T. Sem – II Microprocessor Architecture

1. 8085 has 5 hardware Interrupt and ------ software interrupt.
    a) 5
    b) 4
    c) 6
    d) 8
2. ---------- holds the opcode of instruction that is decoded and executed
    a) Program counter
    b) Flag registers
    c) Stack pointer
    d) Instruction registers
3. The processing speed of microprocessor depends upon clock ----------.
    a) Processing capability
    b) Clock frequency
    c) Word length
    d) Width of data bus
4. In Pentium processor, The logical address in protected mode operation have 16 bit selector and 32 bit ----------.
    a) DIR
    b) Page
    c) Offset
    d) Frame
5. ---------- hold the destination data for string instruction.
    a) EBP
    b) EDI
    c) ESI
    d) ESP
6. The control word register consist of ---- latches use to store bit pattern given by the programmer.
    a) 4
    b) 8
    c) 10
    d) 12
7. ---------- instruction will load the PC with C200 and the processor will fetch instruction address from this location.
    a) JCOND C200H
    b) RST C200H
    c) JMP C200H
    d) CALL C200H
8. To set carry flag we use ---------- instruction.
    a) STA
    b) SCT
    c) SCA
    d) STC

9. When RMI instruction is executed then status of masking is loaded at Bit ----------.
    a) D3 to D0
    b) D7 to D4
    c) D5 to D2
    d) D4 to D1
10. In Pentium pro processor if PSE bit=0 indicate page size is ---------.
    a) 1KB
    b) 2KB
    c) 4KB
    d) 8KB
11. The ---------- unit in Sun Super SPARC, dynamically select "a group" up to three instruction in each cycle.
    a) Cache
    b) MMU
    c) Floating point
    d) Integer
12. The number of T states required to perform an operation is called as ---------- cycle.
    a) Machine
    b) Operand
    c) Fetch
    d) Opcode
13. When the accumulator is high order register and flag registers are low order registers then it is called as ----------.
    a) Stack pointer
    b) Program status word
    c) Serial I/O control group
    d) Interrupt control
14. The interrupt vectored location for ---------- is 003C H.
    a) Trap
    b) RST 7.5
    c) RST 5.5
    d) RST 6.5
15. In the ----------,timer gives only one cycle of square wave,the output remains high for the ½ count and low for the ½ count.
    a) Mode 0
    b) Mode 1
    c) Mode 2
    d) Mode 3
16. The combination of Opcode and Operand, that can be used to instruct the system is called as ----------.
    a) Bus
    b) Routine
    c) Instruction
    d) Subroutine

17. ---------- is a used to represent BCD data.
    a) Word
    b) Byte
    c) Nibble
    d) Tri-state
18. In ----------, bit D0,D1 and D2 are used for handshake signals for port A.
    a) Status word
    b) Control word register
    c) Timer
    d) Counter status register
19. ---------- deferment the content of memory location address by HL register pair by 1.
    a) DCR R
    b) DCR M
    c) DCX Rp
    d) DCX M
20. Three byte instruction are used to specify ---------- address or memory location with the instruction.
    a) 8 bit
    b) 16 bit
    c) 32 bit
    d) 64 bit
21. Temporary data register is Use to provide operands to -----.
    a) Program counter
    b) ALU
    c) Address/Data buffer
    d) Stack pointer
22. ----------8086 mode is dynamic mode where in sense that processor can switch repeatedly and rapidly between v86 and protected mode.
    a) Real
    b) SMM
    c) Virtual
    d) Protected
23. In CPUID, the ---------- consist of Intel architecture family identifier, model identifier, stepping ID and processor type.
    a) Cache information
    b) Feature information
    c) Reserved
    d) Version information
24. IE flip-flop=0 operation will be carried out when ------ instruction get executed.
    a) NOP
    b) HLT
    c) EI
    d) DI

25. LHLD 4000H,instruction load the HL pair from memory location 4000H and----------.
    a) 3000H
    b) 5000H
    c) 3900H
    d) 4001H